REMARKS

Claims 19 and 38 have been amended. Claim 37 has been canceled. Claims 24-34 and 36 were previously canceled. Claim 41 has been added. Claims 1-23, 35, and 38-41 are pending in the application. No new matter has been added. Applicants reserve the right to pursue the original claims and other claims in this and other applications.

Claim 19 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Yang (U.S. Patent No. 6,498,387). The rejection is respectfully traversed.

Amended claim 19 recites a method of making semiconductor device packages. The method includes the acts of "aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape; subsequently, attaching said semiconductor wafer to said dielectric tape; connecting said semiconductor devices in said wafer to ball grid arrays on said dielectric tape; and simultaneously dicing said wafer and said dielectric tape." Applicants respectfully submit that Yang fails to disclose every limitation of claim 19.

Yang relates to a wafer level package and the processing of the wafer level package. Yang, however, discloses an adhesive material 11 that is coated on a wafer 5; then a curing step is performed to harden the adhesive material 11; and then a plurality of pad openings are formed in the adhesive material 11 and aligned to the pads 13 of the dies. (Yang, col. 3, lines 53-66).

Applicants respectfully submit that Yang discloses a method of wafer level packaging wherein openings are formed in the adhesive material after it has been attached to the wafer, and that the formation of the openings are in alignment with the pads of the dies. On the other hand, amended claim 19 recites "aligning a plurality of

semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape; subsequently, attaching said semiconductor wafer to said dielectric tape; [and] connecting said semiconductor devices in said wafer to ball grid arrays on said dielectric tape." Therefore, Yang does not disclose the claim 19 method. Applicants respectfully request the withdrawal of the rejection and the allowance of claim 19.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang in view of Gaynes et. al. (U.S. Patent No. 6,165,885). The rejection is respectfully traversed.

Claim 20 depends from claim 19. For at least the reasons discussed above, Yang fails to disclose, teach or suggest all of the limitations of claim 19. The Office Action relies on Gaynes for teaching a wafer being optically aligned with respect to said dielectric tape. (Office Action at page 3). The alleged teaching, however, does not cure the deficiencies of Yang. Therefore, even when considered in combination, Yang and Gaynes fail to teach or suggest all limitations of claims 19 and 20. Applicants respectfully request the withdrawal of the rejection and the allowance of claim 20.

Claims 21-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang in view of Smith (U.S. Patent No. 6,300,149). The rejection is respectfully traversed.

Claims 21-23 depend from claim 19. For at least the reasons discussed above, Yang fails to disclose, teach or suggest all of the limitations of claim 19. The Office Action relies on Smith for disclosing "[a] wafer ... magnetically aligned with respect to said dielectric tape," "oppositely charged magnetic elements ... provided on said wafer and said tape," and "the step of locating a magnetic ring in a charged slot." These features of Smith, however, do not cure the deficiencies of Yang. Therefore, even when

considered in combination, Yang and Smith fail to teach or suggest all limitations of claims 19, 21, 22, and 23. Applicants respectfully request the withdrawal of the rejection and the allowance of the claims.

Claims 1-18, 35, and 37-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohsawa et. al. (U.S. Patent No. 6,020,626) in view of Yang. The rejection is respectfully traversed.

Claim 1 recites a method of making semiconductor device packages. The method includes the steps of "forming conductive traces in contact with a top surface of a dielectric substrate; subsequently, forming a layered assembly by attaching a wafer to said dielectric substrate, such that said conductive traces are in electrical communication with semiconductor devices in said wafer; forming input/output devices in contact with said conductive traces; testing semiconductor devices in said wafer; and subsequently, dicing said layered assembly." Applicants respectfully submit that the cited combination fails to disclose, teach, or suggest the claim 1 invention.

The Office Action states that Ohsawa discloses the acts of forming conductive structures 10b in contact with a top surface of a dielectric substrate 8; subsequently, forming a layered assembly by attaching a wafer 11b to said dielectric substrate 8, such that said conductive traces 10b are in electrical communication with semiconductor devices in said wafer 11b; forming input/output devices 12b in contact with said conductive traces 10b. (Office Action at page 5).

Applicants respectfully submit that Ohsawa relates to a semiconductor package in which a semiconductor chip is joined with a new lead frame to make up a structure having an ultra-number of pins. (Ohsawa, col. 1, lines 4-6). Specifically,

Ohsawa discloses a method of packaging individual semiconductor devices. Ohsawa fails to disclose or suggest the use of an entire wafer consisting of several semiconductor chips. In Figure 10, Ohsawa discloses a method in which each individual semiconductor chip 2 is dye-bonded via the adhesive layer 5 to the insulating film 11a. (Ohsawa, col. 9, lines 49-51). Ohsawa fails to disclose forming a layered assembly by attaching a wafer to a dielectric substrate, where there are semiconductor devices in the wafer, as recited in claim 1. Ohsawa only discloses that an individual semiconductor chip 2 is bonded to an insulating film 11a by means of an adhesive layer 5. Accordingly, Ohsawa fails to disclose the limitations "forming conductive traces in contact with a top surface of a dielectric substrate; [and] subsequently, forming a layered assembly by attaching a wafer to said dielectric substrate, such that said conductive traces are in electrical communication with semiconductor devices in said wafer," as recited in claim 1.

Furthermore, the Office Action admits that Ohsawa does not disclose "forming input/output devices in contact with said conductive traces; testing semiconductor devices in said wafer; and subsequently, dicing said layered assembly," as recited in claim 1. (Office Action at 7). In fact, Ohsawa is silent about testing semiconductor devices in any way. Accordingly, Ohsawa fails to disclose every limitation of claim 1.

In an effort to remedy the deficiencies of Ohsawa, the Office Action relies on Yang as disclosing the acts of "testing semiconductor devices in said wafer; and subsequently, dicing said layered assembly," as recited in claim 1. Yang, however, does not disclose a method of making semiconductor device packages, comprising the acts of "forming conductive traces in contact with a top surface of a dielectric substrate; [and] subsequently, forming a layered assembly by attaching a wafer to said dielectric

substrate, such that said conductive traces are in electrical communication with semiconductor devices in said wafer," as recited in claim 1.

As such, Yang fails to cure the deficiencies of Ohsawa and thus, the combination fails to disclose, teach, or suggest every limitation recited in claim 1. Accordingly, claim 1 is allowable over the combination of the Ohsawa and Yang. Claims 2-10 depend from claim 1 and are allowable along with claim 1.

Claim 11 recites a method of making semiconductor device packages. The method comprises "providing conductive structures in contact with a top surface of a dielectric substrate; subsequently, forming a layered assembly by attaching a semiconductor wafer and a stiff metal layer to said dielectric substrate; placing ball grid arrays in contact with said conductive structures; electrically connecting semiconductor devices in said semiconductor wafer to said ball grid arrays; determining whether the wafer contains a defective semiconductor device; and subsequently, dicing said layered assembly." Applicants respectfully submit that claim 11 is allowable over the cited combination.

As with claim 1, the Office Action states that Ohsawa discloses the acts of forming conductive structures 10b in contact with a top surface of a dielectric substrate 8; subsequently, forming a layered assembly by attaching a wafer 11b to said dielectric substrate 8, such that said conductive traces 10b are in electrical communication with semiconductor devices in said wafer 11b; forming input/output devices 12b in contact with said conductive traces 10b. (Office Action at page 5).

As discussed above, Ohsawa discloses a method of packaging <u>individual</u> semiconductor devices. Ohsawa fails to disclose, teach, or suggest the use of an entire wafer consisting of <u>several</u> semiconductor chips. Accordingly, Ohsawa fails to disclose

"forming a layered assembly by attaching a semiconductor wafer ... to said dielectric substrate; placing ball grid arrays in contact with said conductive structures; [and] electrically connecting semiconductor devices in said semiconductor wafer to said ball grid arrays," as recited in claim 11.

In addition, the Office Action admits that Ohsawa does not disclose testing semiconductor devices through input/output devices and subsequently dicing the layered assembly. (Office Action at 7). In fact, Ohsawa is silent about testing semiconductor devices in any way. Accordingly, Ohsawa fails to disclose the exemplary method as recited in claim 11.

The Office Action cites to Yang as disclosing the acts of "determining whether the wafer contains a defective semiconductor device; and subsequently, dicing said layered assembly." Yang, however, is silent on determining whether the wafer contains a defective semiconductor device and then dicing said layered assembly. Yang discloses the occurrence of a sawing process after a wafer-level test. (Yang, col. 2, lines 48-50).

Moreover, the Office Action relies on Yang for disclosing "a stiff metal layer," as recited in claim 11. Applicants respectfully submit, however, that Yang fails to disclose, teach, or suggest the use of a metal layer in wafer-level packaging of semiconductor devices, as recited in claim 11.

Applicants respectfully submit that whether considered alone or in combination, neither Ohsawa nor Yang disclose, teach, or suggest the method of claim 11. Accordingly, claim 11 is allowable over the combination of the Ohsawa and Yang. Claims 12-18 depend from claim 11 and are allowable along with claim 11.

Claim 35 recites a method of handling a plurality of semiconductor devices arrayed in a semiconductor wafer. The method includes the steps of "adhering said wafer to a flexible substrate; connecting said semiconductor devices to respective ball grid arrays located on said flexible substrate; testing said semiconductor devices through said ball grid arrays; and subsequently, singulating packages from said wafer and said substrate." Applicant respectfully submits that the cited combination fails to disclose, teach, or suggest the claim 35 invention.

The Office Action states that Ohsawa discloses the act of connecting said semiconductor devices to respective ball grid arrays located on said substrate. As discussed above, Ohsawa only discloses packaging of individual semiconductor devices, and not a plurality of semiconductor devices arrayed in a semiconductor wafer, as recited in claim 35.

Additionally, the Office Action admits that Ohsawa does not disclose testing semiconductor devices through input/output devices and subsequently dicing the layered assembly, as recited in claim 35. (Office Action at 7). In fact, Ohsawa is silent about testing semiconductor devices in any way. Accordingly, Ohsawa fails to disclose every limitation of claim 35.

The Office Action relies on Yang for disclosing semiconductor device testing; however, Yang is silent on "testing said semiconductor devices through said ball grid arrays; and subsequently, singulating packages from said wafer and said substrate," as recited in claim 35.

The Office Action also admits that Ohsawa fails to disclose "adhering said wafer to a flexible substrate," as recited in claim 35. (Office Action at 7). Instead, the Office Action relies on Yang for disclosing this limitation. (Office Action at page 7).

Applicants respectfully submit that Yang does not disclose, teach, or suggest adhering a wafer to a flexible substrate. In fact, Yang discloses the lamination of glass on one side of the wafer and on the opposite side of the wafer an epoxy is coated by means of a vacuum coating process; and then, a curing step is performed to harden the epoxy. (Yang, Abstract). As such, Yang does not disclose adhering a flexible substrate to a wafer, as recited in claim 35.

As discussed above, neither Ohsawa nor Yang, when considered alone or in combination teach, disclose, or suggest every limitation of claim 35. Accordingly, claim 35 is allowable over the combination of the Ohsawa and Yang. Claims 38 and 41 depend from claim 35 and are allowable along with claim 35. Claims 39 and 40 depend from claim 19. For at least the reasons discussed above, Yang fails to disclose, teach or suggest all limitations of claim 19. Ohsawa also fails to disclose, teach, or suggest the claim 19 method. Accordingly, claims 39 and 40 are allowable for at least these same reasons. Applicants respectfully request the withdrawal of the rejection and the claims allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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